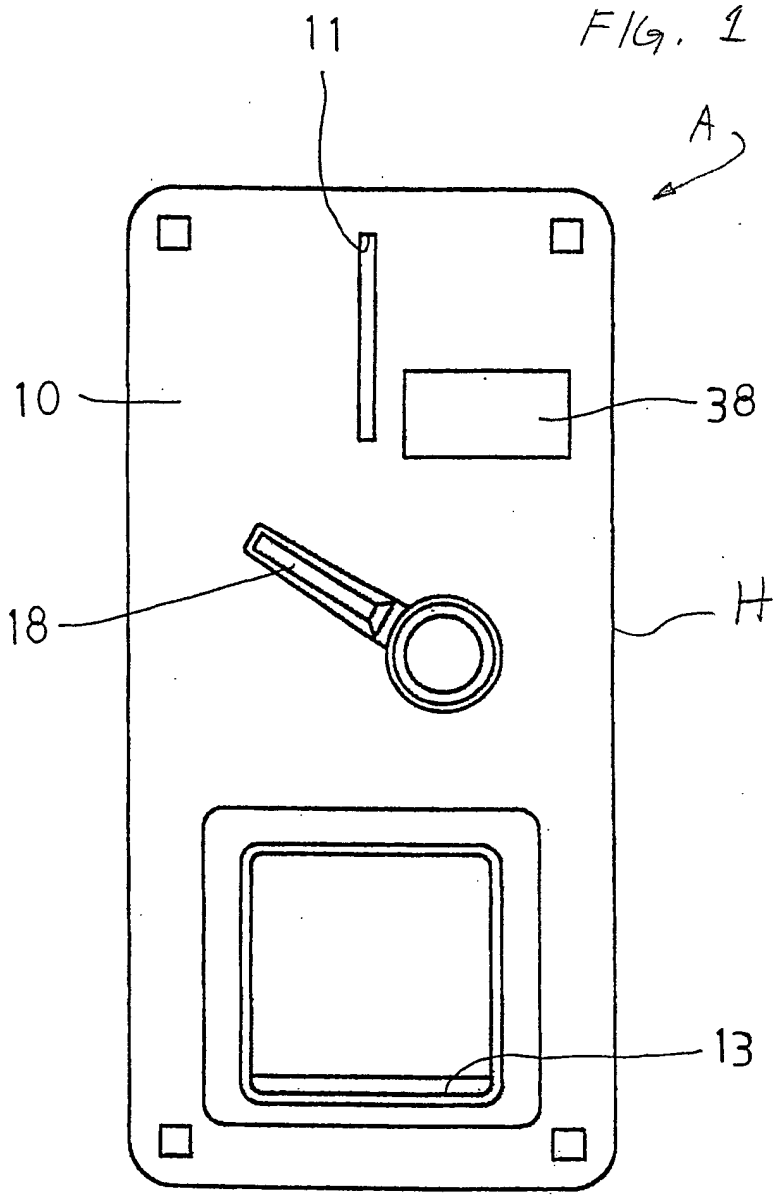



Fig. 1

FIG. 2

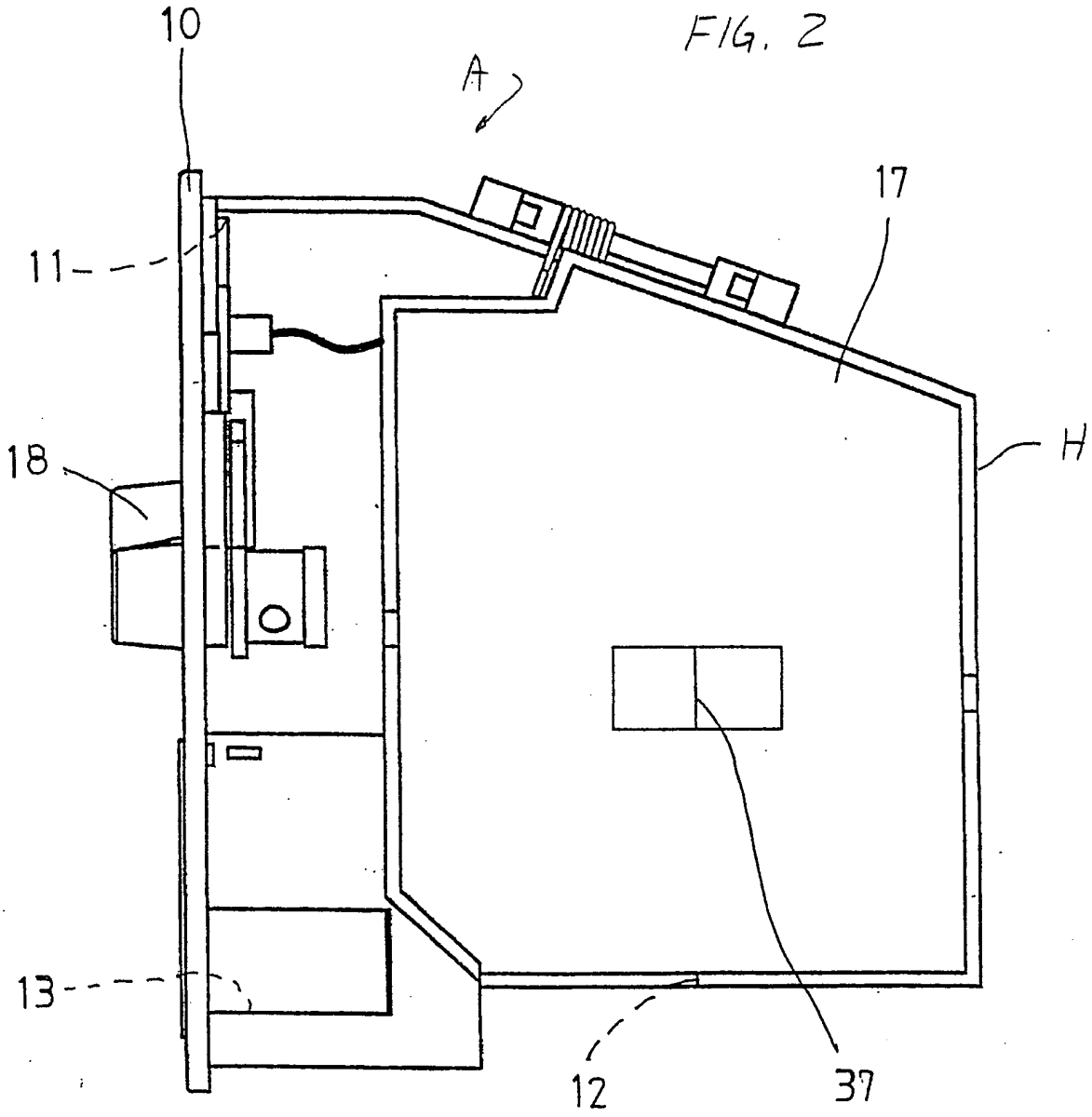


FIG. 3

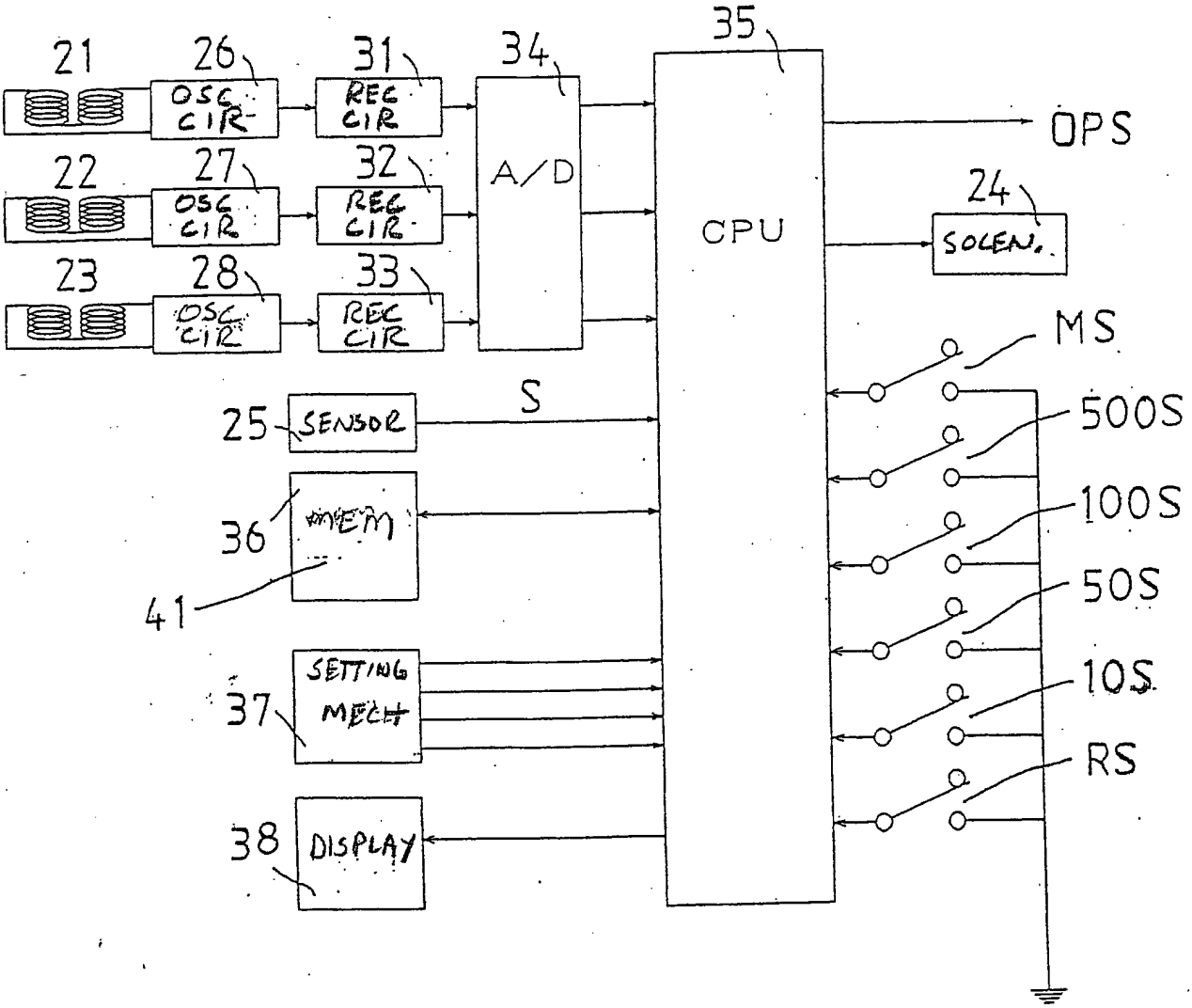

21
26
OSC CIR
31
REC CIR
34
A/D
35
CPU
OPS
22
27
OSC CIR
32
REC CIR
24
SOLEN.
23
28
OSC CIR
33
REC CIR
MS
25
SENSOR
S
500S
36
MEM
100S
41
50S
SETTING MECH
37
10S
RS
38
DISPLAY

FIG. 4

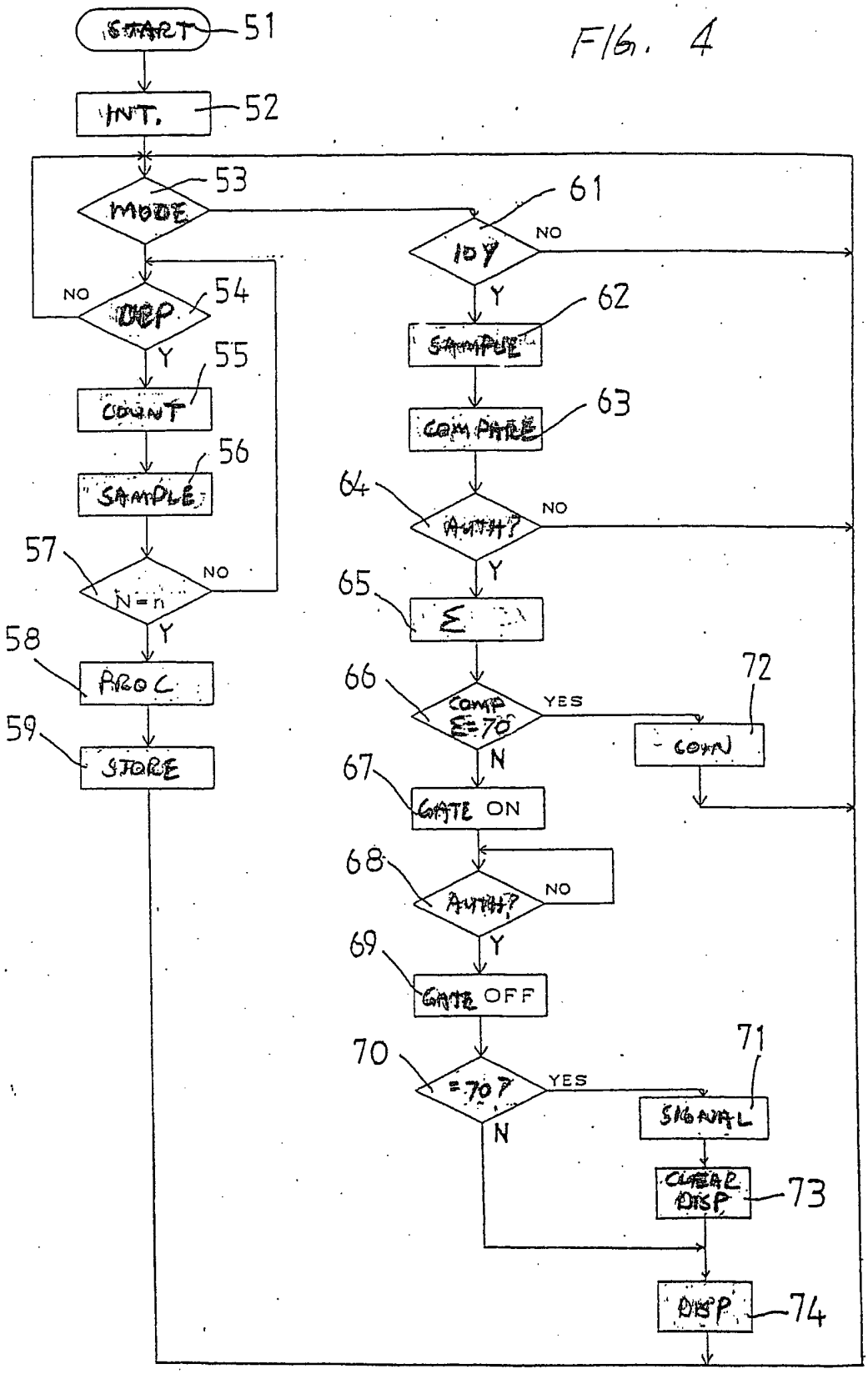
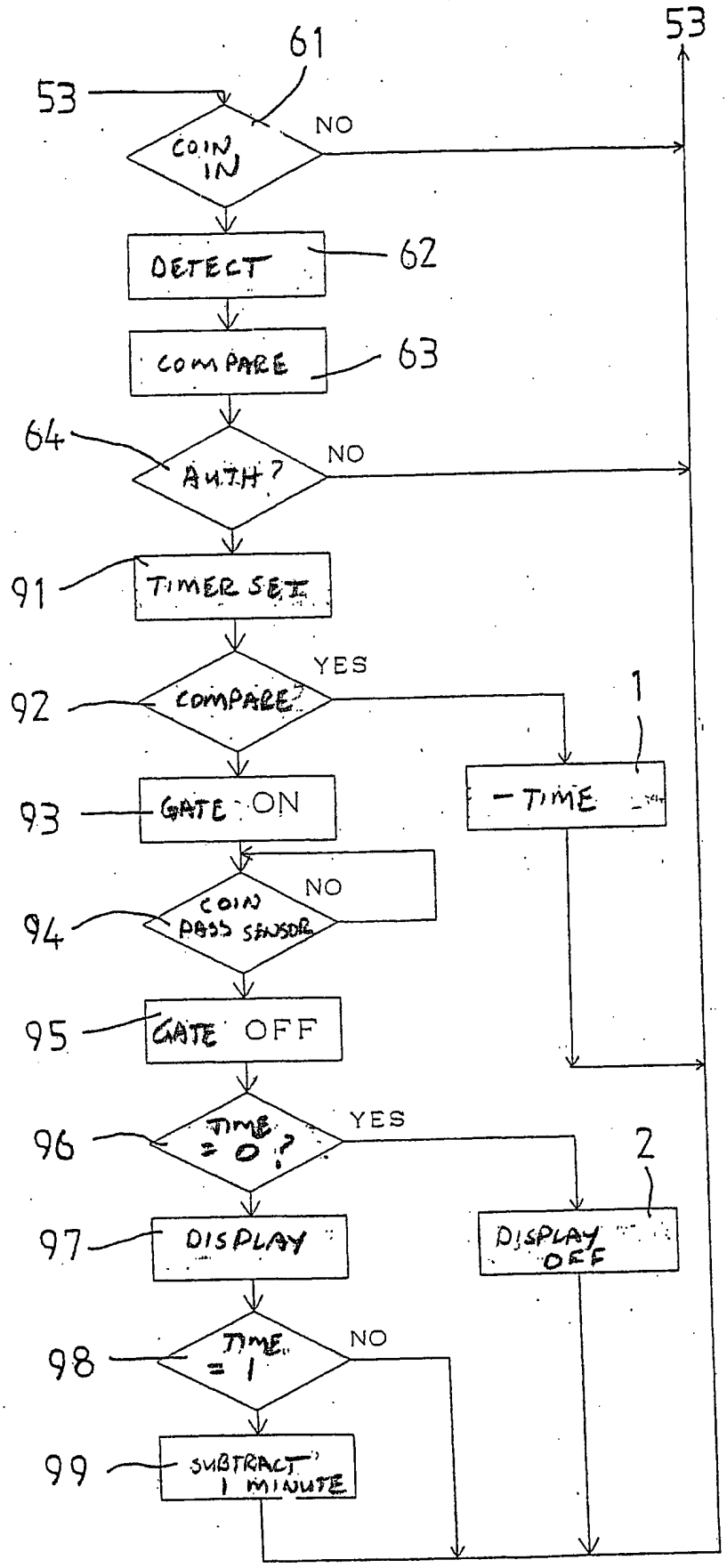

START
51
INT.
52
MODE
53
61
ID?
NO
Y
DEP
54
NO
Y
62
SAMPLE
COUNT
55
63
COMPARE
SAMPLE
56
64
AUTH?
NO
Y
57
N=n
NO
Y
65
Σ
58
PROC
66
COMP Σ=70
YES
72
COUNT
59
STORE
N
67
GATE ON
68
AUTH?
NO
Y
69
GATE OFF
70
=70?
YES
71
SIGNAL
N
CLEAR DISP
73
DISP
74

FIG. 5


53
61
53
COIN IN
NO
DETECT
62
COMPARE
63
64
AUTH?
NO
91
TIMER SET
YES
92
COMPARE
1
-TIME
93
GATE ON
NO
94
COIN PASS SENSOR
95
GATE OFF
96
TIME = 0 ?
YES
2
97
DISPLAY
DISPLAY OFF
98
TIME = 1
NO
99
SUBTRACT 1 MINUTE